3.2 A 375mW Quadrature Bandpass ΔΣ ADC with 90dB DR and 8.5MHz BW at 44MHz

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Television is one of the first applications for broadband communications and continues to be one of the largest. Numerous legacy analog standards, together with the new and increasing number of digital standards, provide the impetus for developing a universal receiver which relies on DSP for the channelization and decoding operations. The receiver architecture shown in Fig. 3.2.1 has the required flexibility as well as a low component count [1].

The ADC in a universal TV receiver must support a bandwidth of f_B = 8MHz (the channel bandwidth in Europe) and an SNR of 55dB (the requirement for "perfect picture" in analog TV). However, additional demands are often placed on the ADC to simplify the receiver design. In particular, the ADC's dynamic range requirement is usually much higher than the above minimum in order to accommodate interferers, to reduce AGC range, and to minimize the ADC's impact on the overall system NF. In the proposed system, these three considerations lead to a DR specification of 83dB and a full-scale AGC range of 12dB. Similarly, ±250kHz frequency resolution in the first LO synthesizer pushes the bandwidth requirement from 8 to 8.5MHz.

The f_0=44MHz IF and the quadrature nature of the ADC input are dictated by the receiver architecture and associated frequency-planning. As a result, a quadrature bandpass ADC fits naturally into the system. Using a sampling rate of $f_s=6f_0=264$MHz facilitates digital down-conversion of the ADC data while providing a reasonably high oversampling ratio of OSR=f_s/f_B=31. Note that the OSR of a quadrature system is twice that of a real system operating with the same bandwidth and sample rate [2]. The 264MHz ADC clock is conveniently obtained by dividing down the second LO.

As shown in Fig. 3.2.2, the continuous-time quadrature converter contains four active-RC resonator stages connected in a modified feed-forward topology. Three of the resonators implement positive-frequency NTF zeros, while the fourth implements a negative-frequency NTF zero. The latter resonator somewhat degrades the effectiveness of the noise-shaping, but provides the necessary robustness in the presence of I/Q path mismatch [2]. In order to reduce hardware requirements, state rotation (scaling by $e^{j\theta}$) is used to make as many feedback coefficients as possible real. In particular, the first feedback coefficient is real and thus DAC1 is implemented with a pair of 16-element current-mode DACs. A direct feedback path to the input of the quantizer (via DAC3) allows complete control over the modulator's NTF. State rotation is not possible for the direct feedback coefficient and so this coefficient is fully complex. Nonetheless, two real DACs suffice for this coefficient since the DACs have voltage-mode outputs, which can be coupled to both the I and the Q summation amplifiers simultaneously.

One unusual feature of the topology is the use of DAC2 at the input of the final resonator. Although DAC2 is not needed from a purely theoretical perspective, DAC2 alleviates the extreme sensitivity to the feed-forward coefficients caused by the accumulated attenuation of the preceding resonators at $-f_0$. The addition of DAC2 is also responsible for a notch in the modulator's signal transfer function at $-f_0$; this notch relaxes the degree of quadrature needed in the digital $f_s/6$ signal which mixes the ADC's output to baseband.

As indicated in Fig. 3.2.2, capacitors are used in the summation amplifier to achieve high-speed summation with minimal phase shift. The use of ac-coupling is possible since the signals of interest are at moderately high frequencies, but care must be taken to ensure that a dc feedback path is present and has the correct magnitude and phase. Resistive connections to DAC3's outputs are used for this purpose.

As shown in Fig. 3.2.3, the ADC's input is taken in current form. A low ADC input impedance minimizes the voltage swing at the output of the quadrature mixer, thereby minimizing distortion from the mixer. In the event of modulator overload or reset, a current attenuator shunts the ADC's input, providing a gentle start-up and allowing the modulator to reliably recover from an overload condition. The 60Ω series resistors in the attenuator prevent shorting of the op amps' input terminals when the attenuator is activated.

The resistors and capacitors of the first resonator are both programmable. The 5b resistor code is set in accordance with the full-scale setting (which is programmable in 1dB steps over a 12dB range), while the 9b capacitor code sets the resonant frequency. Tuning of all resonators is accomplished at power-up by converting each resonator in turn into an oscillator and adjusting its capacitor code until the desired oscillation frequency is obtained.

Figure 3.2.4 shows the output PSD for zero input along with the measured and the theoretical NTF (scaled to account for the noise bandwidth and theoretical quantization noise power) when the ADC full-scale is at maximum. The mean in-band noise floor is -155dBFS/Hz. Figure 3.2.4 also shows the ADC's STF along with measured data. STF peaking is 10dB, but these peaks are not problematic since they lie outside the SAW filter's passband.

Figure 3.2.5 displays the in-band spectrum for a two-tone input at the maximum full-scale setting. The peak amplitude of this signal is -0.5 dBFS, and the IMD products are at -77 dBFS. Figure 3.2.6 plots the observed SNR with a single-tone input as a function of the tone amplitude for both minimum and maximum full-scale settings. The peak SNR and the AGC-free DR are 76 and 85dB, respectively. The DR including the AGC is 90dB, while the image rejection of the ADC is greater than 40dB.

The ADC occupies 2.5mm^2 in a 0.18μm CMOS process and consumes 375mW. All blocks use a 1.8V supply, except for the first resonator and feedback DAC. These two blocks use a 3.3V supply in order to easily interface to the external 3.3V quadrature mixer.

Acknowledgments:
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References:
[1] I. Mehr et al., "A dual-conversion tuner for multi-standard terrestrial and cable reception," *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 340-343, June, 2005.
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[3] N. Yaghini and D. Johns, "A 43mW CT Complex ΔΣ ADC with 23MHz Signal Bandwidth and 68.8dB SNDR," *ISSCC Digest of Technical Papers*, pp. 502-503, Feb., 2005.

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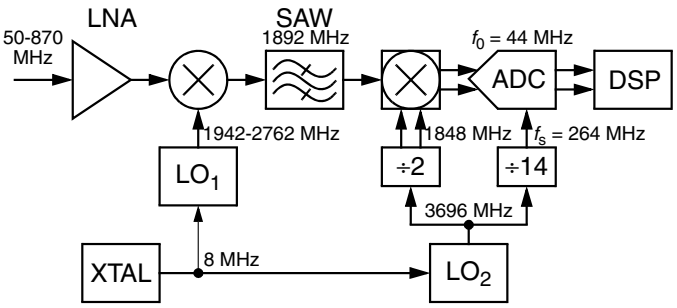

Figure 3.2.1: Universal TV RX architecture and frequency plan.

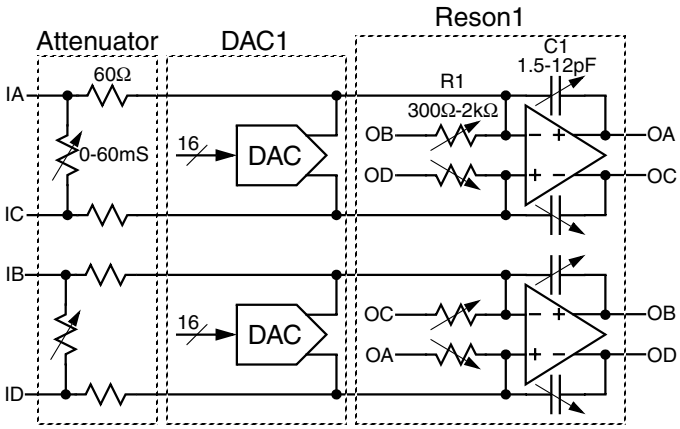

Figure 3.2.3: ADC front-end input attenuator, DAC1 and Reson1.

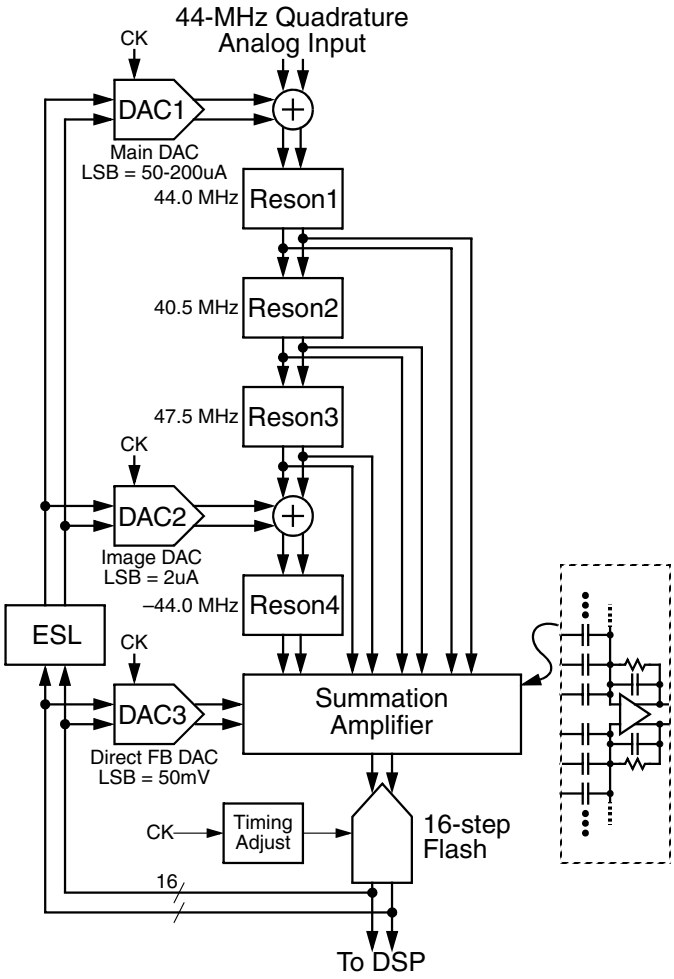

Figure 3.2.2: Quadrature ΔΣ ADC architecture.

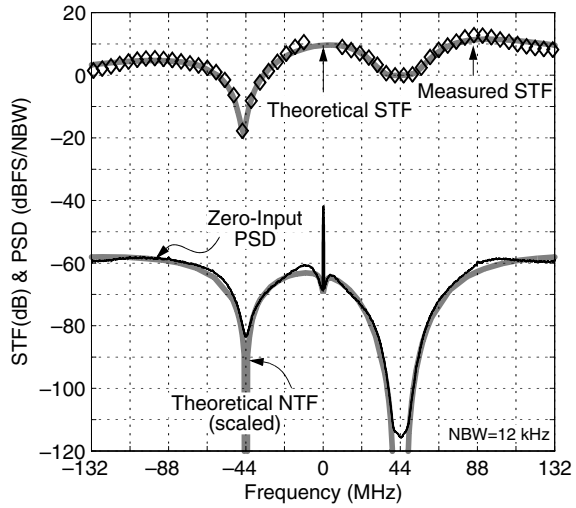

Figure 3.2.4: NTF and STF.

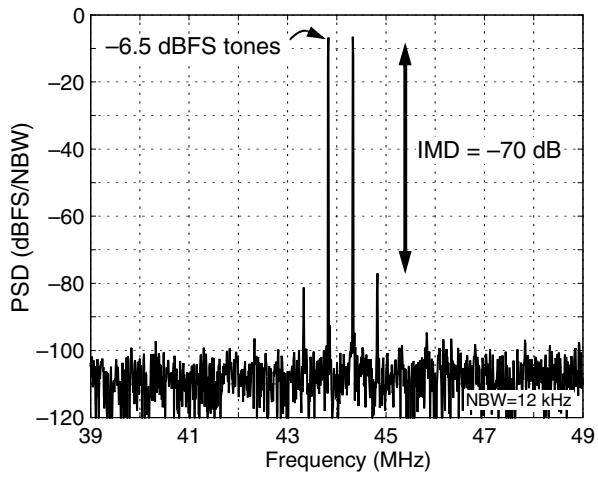

Figure 3.2.5: Two-tone spectrum at maximum full-scale.

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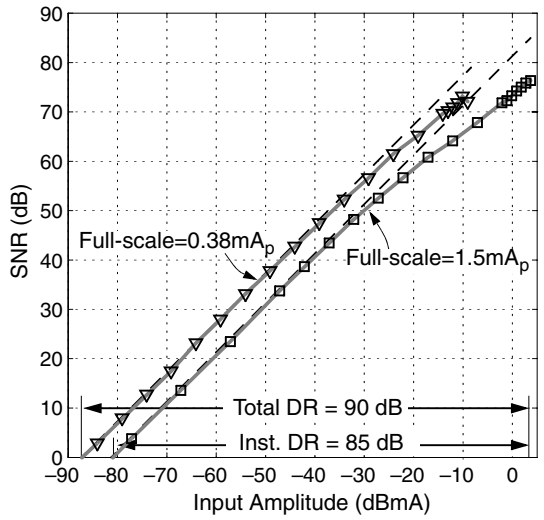

Figure 3.2.6: SNR versus input amplitude.

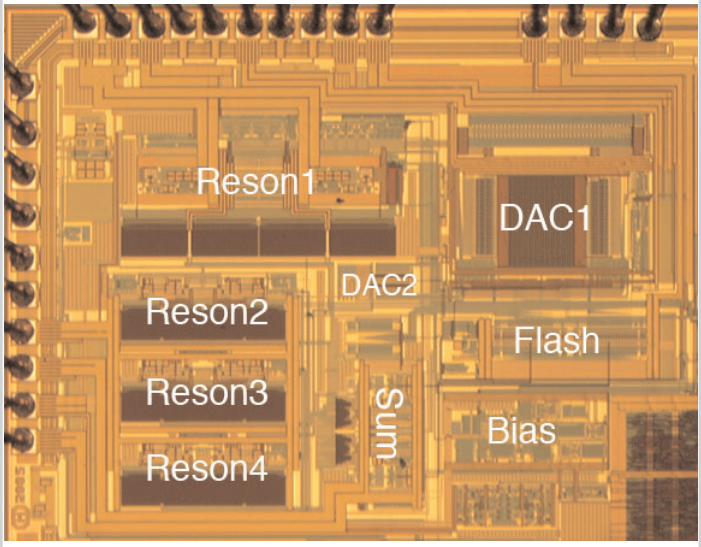

Figure 3.2.7: Chip micrograph.

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